Abstract

An input port is described having an input policing unit that checks if a virtual lane has a sufficient number of credits to carry an input packet received by the input policing unit. The input port also has a request manager that generates a request for the packet to be switched by a switching core. The input port also has a packet Rx unit that stores the packet into a memory by writing blocks of data into the memory. The input port also has a packet Tx unit that receives a grant in response to the request and reads the packet from the memory in response to the grant by reading the blocks of data. The input port also has a pointer RAM manager that provides addresses for free blocks of data to said packet Rx unit and receives addresses of freed blocks of data from said packet Tx unit.